

**WHAT IS CLAIMED IS:**

1 1. An output buffer, comprising:

2 a first circuit coupled between a first power line and a  
3 pad; and

4 a second circuit coupled between a second power line and  
5 the pad, comprising:

6 a resistor constructed by a well region of a second  
7 conductivity type deposited on a substrate of a first  
8 conductivity type, the resistor comprising a first  
9 end and a second end, the first end being a doped  
10 region of the second conductivity type at least  
11 partially overlapping the well region and coupled to  
12 the pad;

13 a first doped region of the first conductivity type,  
14 electrically floated in the well region; and

15 an electrostatic discharge protection component,  
16 coupled between the second end and the second power  
17 line.

1 2. The output buffer of claim 1, wherein the second circuit  
2 further comprises a capacitor coupled between the pad  
3 and the first doped region.

1 3. The output buffer of claim 1, wherein the electrostatic  
2 discharge protection element is a MOS transistor  
3 comprising a gate, a drain and a source, the drain being  
4 coupled to the second end of the resistor 0 and the  
5 source being coupled to the second power line.

1 4. The output buffer of claim 3, wherein the drain and the  
2 source are respectively comprised of a second doped  
3 region of the second conductivity type and a third doped  
4 region of the second conductivity type.

1 5.The output buffer of claim 3, wherein the gate is  
2 coupled to a signal source.

1 6.The output buffer of claim 3, wherein the gate is  
2 coupled to the second power line.

1 7.The output buffer of claim 3, wherein the MOS transistor  
2 is a finger-shaped MOS.

1 8.The output buffer of claim 1, wherein the first and the  
2 second ends are respectively comprised of a fourth doped  
3 region of the second conductivity type and a fifth doped  
4 region of the second conductivity type.

1 9.The output buffer of claim 8, wherein the first doped  
2 region is deposited between the fourth doped region and  
3 the fifth doped region.

1 10. The output buffer of claim 8, wherein the  
2 electrostatic discharge protection component is a MOS  
3 transistor of the second conductivity type, the MOS  
4 transistor being comprised of a gate, a drain, a source,  
5 and a substrate, the drain being composed of the fifth  
6 doping region and the source being coupled to the second  
7 power line.

1 11. The output buffer of claim 8, wherein the first doping  
2 region interlaces with the fourth doped region.

1 12. The output buffer of claim 8, wherein the first doped  
2 region is in contact with the fourth doped region.

1 13. The output buffer of claim 1, wherein, during an ESD  
2 event, the first doped region is coupled to the first  
3 end.

1 14. The output buffer of claim 1, wherein the substrate is  
2 coupled to the second power line through the sixth doped  
3 region.

1 15. An electrostatic discharge protection circuit, coupled  
2 between a first pad and a second pad, comprising:  
3 a resistor consisted of a well region of a second  
4 conductivity type, deposited on the substrate of a  
5 first conductivity type, and coupled to the first pad;  
6 a first doped region of the first conductivity type,  
7 electrically floated in the well region; and  
8 a electrostatic discharge protection component, coupled  
9 between the well region and the second pad.

1 16. The electrostatic discharge protection circuit of  
2 claim 15, wherein, during an ESD event, the first doped  
3 region is coupled to the first pad.

1 17. The electrostatic discharge protection circuit of  
2 claim 15, wherein the first pad is coupled to an output  
3 port and the second pad is coupled to a power line.

1 18. The electrostatic discharge protection circuit of  
2 claim 15, wherein the first and the second pads are  
3 respectively coupled to a first and a second power  
4 lines.

1 19. The electrostatic discharge protection circuit of  
2 claim 15, wherein the electrostatic discharge protection  
3 component is a MOS transistor of the second conductivity

4 type, the MOS transistor comprising a gate, a drain, a  
5 source and a substrate, the drain being coupled to the  
6 resistor and the source being coupled to the second pad.

1 20. The electrostatic discharge protection circuit of  
2 claim 19, wherein the gate is coupled to the second pad.

1 21. The electrostatic discharge protection circuit of  
2 claim 19, further comprising a delaying circuit which  
3 consists of a resistor and a capacitor connected in  
4 series, the delaying circuit being coupled between the  
5 first pad and the second pad, the gate being coupled to  
6 a node for connecting the resistor and the capacitor.

1 22. The electrostatic discharge protection circuit of  
2 claim 19, wherein the drain is coupled to a first pad.

1 23. The electrostatic discharge protection circuit of  
2 claim 15, wherein the electrostatic discharge protection  
3 component is a field oxide device.

1 24. The electrostatic discharge protection circuit of  
2 claim 23, wherein the field oxide device comprises a  
3 second doped region of the second conductivity type and  
4 a third doped region of the second conductivity type,  
5 the second doped region and the third doped region being  
6 formed on the substrate.

1 25. The electrostatic discharge protection circuit of  
2 claim 24, wherein the field oxide device further  
3 comprises a field oxide layer formed between the second  
4 and the third doped regions.

1 26. The electrostatic discharge protection circuit of  
2 claim 15, wherein the substrate is coupled to the second

3        pad via a sixth doped region of the first conductivity  
4        type.

1        27. The electrostatic discharge protection circuit of  
2        claim 26, wherein the sixth doped region partly embraces  
3        the electrostatic discharge protection circuit.

1        28. The electrostatic discharge protection circuit of  
2        claim 26, wherein a seventh doped region of the second  
3        conductivity type is formed between the sixth doped  
4        region and the well region.

1        29. The electrostatic discharge protection circuit of  
2        claim 15, wherein the first conductivity type is n-type  
3        and the second conductivity type is p-type.

1        30. The electrostatic discharge protection circuit of  
2        claim 15, wherein the first conductivity type is a p-  
3        type and the second conductivity type is an n-type.

1        31. An output buffer, comprising:  
2        a first circuit, coupled between a first power line and  
3        a pad; and  
4        a second circuit coupled between a second power line and  
5        a pad, comprising:  
6        a resistor, comprised of a well region of the second  
7        conductivity type and comprising a first end and a  
8        second end, the first end being a doped region of a  
9        second conductivity type overlapping the well region  
10       and coupled to the pad;  
11       a first doped region of the first conductivity type,  
12       electrically floating in the well region; and  
13       an electrostatic discharge protection component,  
14       coupled between the second end and the second power  
15       line.

1 32. An electrostatic discharge protection circuit, coupled  
2 between a first pad and a second pad, comprising :  
3 a resistor, which consists of a second well region of a  
4 second conductivity type and coupled to the first pad;  
5 a first doped region of a first conductivity type,  
6 electrically floated in the second well region; and  
7 a electrostatic discharge protection component,  
8 deposited on a first well region of a first  
9 conductivity type and coupled between the second well  
10 region and the second pad.

1 33. The electrostatic discharge protection circuit of  
2 claim 32, further comprising a first capacitor coupled  
3 between the first pad and the first doped region.